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Introduction
Transistors
Logic gates
Binary numbers
Memory and clock
Instructions
Loops
Input and output
Conclusion
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Computer Networking Fundamentals | Networking Tutorial for beginners Full Course - Computer Networking Fundamentals | Networking Tutorial for beginners Full Course by Nerd's lesson 223,896 views 2 years ago 6 hours, 30 minutes - In this course you will learn the building blocks of **modern**, network design and function. Learn how to put the many pieces together ...
Understanding Local Area Networking
Defining Networks with the OSI Model
Understanding Wired and Wireless Networks
Understanding Internet Protocol
Implementing TCP/IP in the Command Line
Working with Networking Services
Understanding Wide Area Networks
Defining Network Infrastructure and Network Security
Digital Design & Computer Architecture: Lecture 1: Introduction and Basics (ETH Zürich, Spring 2020) - Digital Design & Computer Architecture: Lecture 1: Introduction and Basics (ETH Zürich, Spring 2020) by Onur Mutlu Lectures 155,494 views 4 years ago 1 hour, 33 minutes - #**computing**, #science #engineering #computerarchitecture #education.
Brief Self Introduction

Current Research Focus Areas
Four Key Directions
Answer Reworded
Answer Extended
The Transformation Hierarchy
Levels of Transformation
Computer Architecture
Different Platforms, Different Goals
Axiom
Intel Optane Persistent Memory (2019)
PCM as Main Memory: Idea in 2009
Cerebras's Wafer Scale Engine (2019)
UPMEM Processing in-DRAM Engine (2019) Processing in DRAM Engine Includes standard DIMM modules, with a large number of DPU processors combined with DRAM chips
Specialized Processing in Memory (2015)
Processing in Memory on Mobile Devices
Google TPU Generation 1 (2016)
An Example Modern Systolic Array: TPU (III)
Security: RowHammer (2014)
Research Directions in RF & High-Speed Design - Research Directions in RF & High-Speed Design by Behzad Razavi (Long Kong) 16,325 views 2 years ago 53 minutes - ... be difficult so difficult that the present **solutions**, cannot solve it and we need some new method and the **solution**, that we propose ...
Lecture 1. Introduction and Basics - Carnegie Mellon - Computer Architecture 2015 - Onur Mutlu - Lecture 1. Introduction and Basics - Carnegie Mellon - Computer Architecture 2015 - Onur Mutlu by Carnegie Mellon Computer Architecture 514,948 views 9 years ago 1 hour, 54 minutes - Lecture 1. Introduction and Basics Lecturer: Prof. Onur Mutlu (http://people.inf.ethz.ch/omutlu/) Date: Jan 12th, 2015 Lecture 1 ...
Intro
First assignment
Principle Design
Role of the Architect
Predict Adapt
Takeaways
Architectural Innovation
Architecture
Hardware
Purpose of Computing
Hamming Distance
Research
Abstraction
Goals
Multicore System
DRAM Banks
DRAM Scheduling
Solution
Drm Refresh
Computer Architecture Complete Course Part 2 - Computer Architecture Complete Course Part 2 by Nerd's lesson 35,800 views 3 years ago 9 hours, 29 minutes - In this course, you will learn to design the **computer architecture**, of complex **modern**, microprocessors.
Memory Dependence Prediction
Superscalar Control Logic Scaling
Out-of-Order Control Complexity MIPS R10000
Sequential ISA Bottleneck
VLIW: Very Long Instruction Word
VLIW Equa
Early VLIW Machines
VLIW Compiler Responsibilities
Loop Execution

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4. Assembly Language & Computer Architecture - 4. Assembly Language & Computer Architecture by MIT OpenCourseWare 677,407 views 4 years ago 1 hour, 17 minutes - Prof. Leiserson walks through the stages of code from source code to compilation to machine code to hardware interpretation and, ...
Intro
Source Code to Execution
The Four Stages of Compilation
Source Code to Assembly Code
Assembly Code to Executable
Disassembling
Why Assembly?
Expectations of Students
Outline
The Instruction Set Architecture
x86-64 Instruction Format
AT&T versus Intel Syntax
Common x86-64 Opcodes
x86-64 Data Types
Conditional Operations
Condition Codes
x86-64 Direct Addressing Modes
x86-64 Indirect Addressing Modes
Jump Instructions
Assembly Idiom 1
Assembly Idiom 2
Assembly Idiom 3
Floating-Point Instruction Sets
SSE for Scalar Floating-Point
SSE Opcode Suffixes
Vector Hardware
Vector Unit
Vector Instructions
Vector-Instruction Sets
SSE Versus AVX and AVX2
SSE and AVX Vector Opcodes
Vector-Register Aliasing
A Simple 5-Stage Processor
Block Diagram of 5-Stage Processor
Intel Haswell Microarchitecture
Bridging the Gap
Architectural Improvements
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Bug Aside
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Instruction Set Architecture (ISA)
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